

## Product Specification

### 10Gb/s Multi-Rate, 10km Single Mode SFP+ Transceiver

#### FTLX1472M3BNL

#### PRODUCT FEATURES

- Hot-pluggable SFP+ footprint
- Up to 10km link length
- 6.14, 8.5 & 9.83 through 11.3 Gb/s
- -5 to 85 °C extended temp. range
- < 1.5W power dissipation,  
< 1.0W with CDR's OFF
- Pb-free / RoHS compliant
- Single 3.3V power supply
- Un-cooled 1310nm DFB laser
- Limiting electrical interface receiver
- Duplex LC connector
- Built-in digital diagnostic functions



#### APPLICATIONS

- 10G NRZ SONET VSR2000-2R1, SDH I-64.1, OTN P1I1-2D1
- 10GBASE-LR/-LW
- 8.5G and 10G Fibre Channel
- 6.144 and 9.83 Gb/s CPRI
- G.709 OTU 1e/2/2e FEC bit rates

Finisar's FTLX1472M3BNL 10Gb/s Enhanced Small Form Factor Pluggable SFP+ transceivers are designed for use in links up to 10km over G.652 single mode fiber, and they are equipped with internal transmitter and receiver retimer units (Clock and Data Recover, or CDR) to comply to SONET/SDH jitter requirements and to enhance host cards' high speed data-signal integrity.

Finisar's FTLX1472M3BNL transceivers are compliant with SFF-8431<sup>1</sup>, SFF-8432<sup>2</sup>, ITU-T G.693 VSR2000-2R1, SDH I-64.1<sup>3</sup>, OTN P1I1-2D1, IEEE 802.3ae 10GBASE-LR/LW<sup>4</sup>, 8.5G and 10G Fiber Channel (1200-SM-LL-L<sup>5</sup>). They also support CPRI bit rates 6.144Gb/s (with CDR's OFF) and 9.83Gb/s with CDR's ON or OFF.

Digital diagnostics functions are available via a 2-wire serial interface, as specified in SFF-8472<sup>6</sup>. The transceivers are Pb-free and RoHS-6<sup>7,8</sup>.

#### PRODUCT SELECTION

**FTLX1472M3BNL**

## I. Pin Descriptions

Pin	Symbol	Name/Description	Ref.
1	V <sub>EET</sub>	Transmitter Ground	1
2	T <sub>FAULT</sub>	Transmitter Fault	2
3	T <sub>DIS</sub>	Transmitter Disable. Laser output disabled on high or open.	3
4	SDA	2-wire Serial Interface Data Line	2
5	SCL	2-wire Serial Interface Clock Line	2
6	MOD_ABS	Module Absent. Grounded within the module	2
7	RS0	Rate Select 0. Used to control the internal CDRs locking modes.	4
8	RX_LOS	Loss of Signal indication. Logic 0 indicates normal operation.	5
9	RS1	Rate Select 1. Used to control the internal CDRs locking modes.	4
10	V <sub>EER</sub>	Receiver Ground	1
11	V <sub>EER</sub>	Receiver Ground	1
12	RD-	Receiver Inverted DATA out. AC Coupled.	
13	RD+	Receiver Non-inverted DATA out. AC Coupled.	
14	V <sub>EER</sub>	Receiver Ground	1
15	V <sub>CCR</sub>	Receiver Power Supply	
16	V <sub>CCT</sub>	Transmitter Power Supply	
17	V <sub>EET</sub>	Transmitter Ground	1
18	TD+	Transmitter Non-Inverted DATA in. AC Coupled.	
19	TD-	Transmitter Inverted DATA in. AC Coupled.	
20	V <sub>EET</sub>	Transmitter Ground	1

### Notes:

- Circuit ground is internally isolated from chassis ground.
- T<sub>FAULT</sub> is an open collector/drain output, which should be pulled up with a 4.7k – 10k Ohms resistor on the host board if intended for use. Pull up voltage should be between 2.0V to V<sub>cc</sub> + 0.3V. A high output indicates a transmitter fault caused by either the TX bias current or the TX output power exceeding the preset alarm thresholds. A low output indicates normal operation. In the low state, the output is pulled to <0.8V.
- Laser output disabled on T<sub>DIS</sub> >2.0V or open, enabled on T<sub>DIS</sub> <0.8V.
- Internally pulled down per SFF-8431 Rev 2.0. See Sec. X for the logic table to use for the internal CDRs locking modes.
- LOS is open collector output. Should be pulled up with 4.7k – 10kΩ on host board to a voltage between 2.0V and 3.6V. Logic 0 indicates normal operation; logic 1 indicates loss of signal.

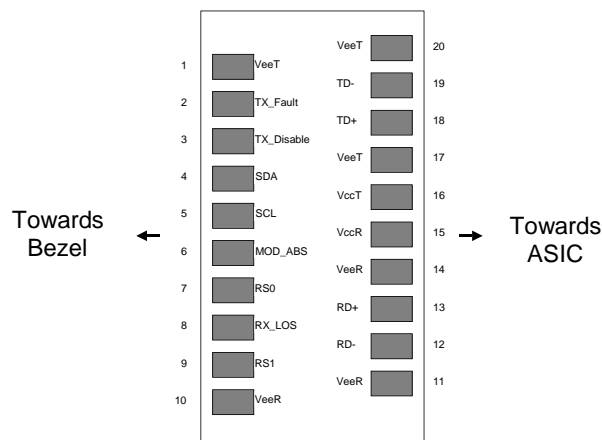


Figure 1. Diagram of Host Board Connector Block Pin Numbers and Names.

**II. Absolute Maximum Ratings**

Exceeding the limits below may damage the transceiver module permanently.

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	V <sub>cc</sub>	-0.5		4.0	V	
Storage Temperature	T <sub>S</sub>	-40		85	°C	
Relative Humidity	RH	0		85	%	1

**Notes:**

1. Non-condensing.

**III. Electrical Characteristics (T<sub>OP</sub> = -5 to 85 °C)**

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	V <sub>cc</sub>	3.14	3.30	3.46	V	
Supply Current	I <sub>cc</sub>		300	430	mA	
Power Dissipation	P <sub>diss</sub>			1.5	W	
<b>Transmitter</b>						
Input differential impedance	R <sub>in</sub>		100		Ω	1
Differential data input swing	V <sub>in,pp</sub>	200		1800	mV	
Transmit Disable Voltage	V <sub>D</sub>	V <sub>cc</sub> -0.8		V <sub>cc</sub>	V	
Transmit Enable Voltage	V <sub>EN</sub>	V <sub>ee</sub>		V <sub>ee</sub> +0.8	V	
<b>Receiver</b>						
Differential data output swing	V <sub>out,pp</sub>	300		850	mV	2
Output rise time and fall time	T <sub>r</sub> , T <sub>f</sub>	28			ps	3
LOS asserted	V <sub>LOS A</sub>	V <sub>cc</sub> -0.8		V <sub>cc</sub>	V	4
LOS de-asserted	V <sub>LOS D</sub>	V <sub>ee</sub>		V <sub>ee</sub> +0.8	V	4
Power Supply Noise Tolerance	V <sub>cc</sub> T/V <sub>cc</sub> R	Per SFF-8431 Rev 3.0			mVpp	5
<b>Power Consumption</b>						
With both CDR's ON	P <sub>consCDRs ON</sub>			1.5	W	
With both CDR's OFF	P <sub>consCDRs OFF</sub>			1.0	W	

**Notes:**

1. Connected directly to TX data input pins. AC coupling from pins into laser driver IC.
2. Into 100Ω differential termination.
3. 20 – 80%. Measured with Module Compliance Test Board and OMA test pattern. Use of four 1's and four 0's sequence in the PRBS 9 is an acceptable alternative. SFF-8431 Rev 3.0.
4. LOS is an open collector output. Should be pulled up with 4.7kΩ – 10kΩ on the host board. Normal operation is logic 0; loss of signal is logic 1.
5. See Section 2.8.3 of SFF-8431 Rev 3.0.

#### IV. Optical Characteristics (T<sub>OP</sub> = -5 to 85 °C, V<sub>CC</sub> = 3.14 to 3.46 Volts)

Parameter	Symbol	Min	Max	Unit	Ref.	
<b>Transmitter (Tx)</b>						
Optical Modulation Amplitude (OMA)	P <sub>OMA</sub>	-5.2		dBm	1	
Average Launch Power	P <sub>AVE</sub>	-6	-1	dBm		
Optical Wavelength	λ	1290	1330	nm		
Side-Mode Suppression Ratio	SMSR	30		dB		
Optical Extinction Ratio	9.83-10.7Gb/s	ER <sub>1</sub>	6	dB		
	11.1-11.3Gb/s	ER <sub>2</sub>	5	dB		
Path Penalty	PP		1	dB		
Transmitter and Dispersion Penalty	TDP <sub>E</sub>		3.2	dB	1	
Average Launch power when Tx is OFF	P <sub>OFF</sub>		-30	dBm		
Tx Jitter 20kHz-80MHz	TX <sub>j1</sub>		0.3	UI	2,3	
Tx Jitter 4MHz – 80MHz	TX <sub>j2</sub>		0.1	UI	2,3	
Relative Intensity Noise	RIN		-128	dB/Hz		
<b>Receiver (Rx)</b>						
Sensitivity (Average Power)	9.83-10.7Gb/s	R <sub>SENS1</sub>		-14.4	dBm	4
	11.1-11.3Gb/s	R <sub>SENS2</sub>		-13.4	dBm	4
Sensitivity (OMA)	6.14,8.5Gb/s	R <sub>SENS3</sub>		-13.8	dBm	5
	10.3-10.5Gb/s	R <sub>SENS4</sub>		-12.6	dBm	
Stressed Sensitivity (OMA)	10.3Gb/s	R <sub>SENS5</sub>		-10.3	dBm	
Overload (Average Power)	P <sub>AVE</sub>		+0.5	dBm		
Optical Center Wavelength	λ <sub>C</sub>	1260	1600	nm		
Receiver Reflectance	R <sub>rx</sub>		-14	dB		
LOS De-Assert	LOS <sub>D</sub>		-17	dBm		
LOS Assert	LOS <sub>A</sub>	-30		dBm		
LOS Hysteresis	LOS <sub>H</sub>	0.5		dB		

**Notes:**

1. For Ethernet and Fiber Channel applications [4], [5]
2. For SONET/SDH applications the jitter specifications are defined as per [9].
3. If the CDRs are in bypass mode, the Tx jitter is compliant to the specification defined in [4].
4. Measured with worst ER=6 dB; BER<10<sup>-12</sup>; 2<sup>31</sup> – 1 PRBS.
5. 6.144Gb/s is supported with both Tx and Rx CDR's in bypass mode.

#### V. General Specifications

Supported bit rates:

- 8.5Gb/s with CDR's ON or OFF.
- 9.8304 through 11.3168 Gb/s with CDR's ON or OFF.
- 6.144G b/s with CDR's OFF.

Parameter	Symbol	Min	Max	Units	Ref.
Optical specifications defined at	BER		10 <sup>-12</sup>	BER	1
Max. Supported Link Length	L <sub>MAX</sub>		10	km	2

**Notes:**

1. Tested with a 2<sup>31</sup> – 1 PRBS pattern.
2. Over G.652 single mode fiber, as per [2], [4], [5].

## VI. Environmental Specifications

The operating temperatures of Finisar FTLX1472M3BNL are shown in the following table

Parameter	Symbol	Min	Max	Units	Ref.
Case Operating Temperature	T <sub>op</sub>	-5	85	°C	
Storage Temperature	T <sub>sto</sub>	-40	85	°C	

## VII. Regulatory Compliance

Finisar transceivers are Class 1 Laser Products and comply with US FDA regulations. These products are certified by TÜV and CSA to meet the Class 1 eye safety requirements of EN (IEC) 60825 and the electrical safety requirements of EN (IEC) 60950. Copies of certificates are available at Finisar Corporation upon request.

## VIII. Digital Diagnostic Functions

Finisar FTLX1472M3BNL SFP+ transceivers support the 2-wire serial communication protocol as defined in the SFP MSA [1]. It is very closely related to the E2PROM defined in the GBIC standard, with the same electrical specifications.

The standard SFP serial ID provides access to identification information that describes the transceiver's capabilities, standard interfaces, manufacturer, and other information.

Additionally, Finisar SFP+ transceivers provide an enhanced digital diagnostic monitoring interface, which allows real-time access to device operating parameters such as transceiver temperature, laser bias current, transmitted optical power, received optical power and transceiver supply voltage. It also defines a sophisticated system of alarm and warning flags, which alerts end-users when particular operating parameters are outside of a factory set normal range.

The SFP MSA defines a 256-byte memory map in E2PROM that is accessible over a 2-wire serial interface at the 8 bit address 1010000X (A0h). The digital diagnostic monitoring interface makes use of the 8 bit address 1010001X (A2h), so the originally defined serial ID memory map remains unchanged. The interface is identical to, and is thus fully backward compatible with both the GBIC Specification and the SFP Multi Source Agreement. The complete interface is described in Finisar Application Note AN-2030: "Digital Diagnostics Monitoring Interface for SFP Optical Transceivers".

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through a 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL, Mod Def 1) is generated by the host. The positive edge clocks data into the SFP transceiver into those segments of the E2PROM that are not write-protected. The negative edge clocks data from the SFP transceiver. The serial data signal (SDA, Mod Def 2) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

For more information, please see the SFP MSA documentation [1], [6] and Finisar Application Note AN-2030. Please note that evaluation board FDB-1027 is available with Finisar ModDEMO software that allows simple to use communication over the 2-wire serial interface.

## IX. Digital Diagnostic Specifications

The digital diagnostic monitors of the FTLX1472M3BNL transceivers are externally calibrated.

Parameter	Symbol	Units	Min	Max	Accuracy	Ref.
<b>Accuracy</b>						
Transceiver temperature	$\Delta DD_{Temp}$	°C	-8	88	$\pm 5^{\circ}C$	1
Transceiver supply voltage	$\Delta DD_{Voltage}$	V	2.8	4.0	$\pm 3\%$	
Transmitter bias current	$\Delta DD_{Bias}$	mA	0	20	$\pm 10\%$	2
Transmitter output power	$\Delta DD_{Tx-Power}$	dBm	-8	+1	$\pm 2dB$	
Receiver average optical input power	$\Delta DD_{Rx-Power}$	dBm	-17	+1.5	$\pm 2dB$	

Notes: 1. Internally measured

2. Accuracy of measured Tx bias current is 10% of the actual bias current from the laser driver to the laser.

## X. Internal CDR's Locking Modes

The FTLX1472M3BNL is equipped with internal CDR units on both the receive and the transmit sides. The host can set the CDR's to lock at 8.5Gb/s, 10G (9.83-11.3Gb/s), or in by-pass mode, by setting the rate select pins or the soft bits (logic OR). The different locking modes are shown in the following logic table:

R/S 0 Logic OR of: pin 7 & bit 110.3	R/S 1 Logic OR of: pin 9 & bit 118.3	CDR's Locking Mode
Low or 0	Low or 0	Both CDR's lock at 8.5Gb/s
Low or 0	High or 1	Tx CDR is in bypass mode. Rx CDR locks at 10G (9.83-11.3Gb/s)
High or 1	Low or 0	Tx & Rx CDR's in bypass mode
High or 1	High or 1	Both CDR's lock at 10G (9.83-11.3Gb/s) The bits 110.3 and 118.3 are set to 1 by default at power-up

The RS0 and RS1 pins are internally pulled-down to ground as per [1]. The soft bits 110.3 and 118.3 are both set to "1" at the transceiver power-up, to select the 10G locking mode by default. The host can change this configuration via the 2-wire communication as described in the SFP MSA [1]. Alternative configurations can be factory set upon request. Please refer to Finisar for additional details.

## XI. SFF-8431 Power-up Sequence

The typical power consumption of the FTLX1472M3BNL will not exceed the limit of 1.5W specified in [1] for a Power Level II device. Moreover, the FTLX1472M3BNL is factory set to power-up directly to its operating conditions, but upon request, it can be factory set to follow the power-up sequence specified in the SFF-8431 for transceivers exceeding 1W. When the transceiver is set into power level mode I, both CDR's are set to the bypass mode.

For additional details please, refer to [1] and Finisar's Application Note AN-2076.

**XII. Mechanical Specifications**

Finisar FTLX1472M3BNL SFP+ transceivers are compatible with the SFF-8432 specification for improved pluggable form factor, and shown here for reference purposes only. Bail color is blue.

ITEM	DIM (mm)	TOL (mm)
A	9.00	±0.3
B	9.60	±0.5
C	11.90	±0.5
D	13.85	±0.15
E	13.65	±0.15
F	2.80	±0.2
G	1.00	±0.2
H	4.00	REF
J	2.00	±0.2
K	56.50	REF
L	1.60	±0.5
M	2.25	±0.1
N	1.80	±0.1
P	37.10	±0.3
Q	9.15	±0.15
R	1.00	±0.1
S	8.55	±0.15
T	47.50	±0.2
V	2.55	±0.1
W	43.00	±0.2
X	14.70	±0.5
Z	0.55	±0.15

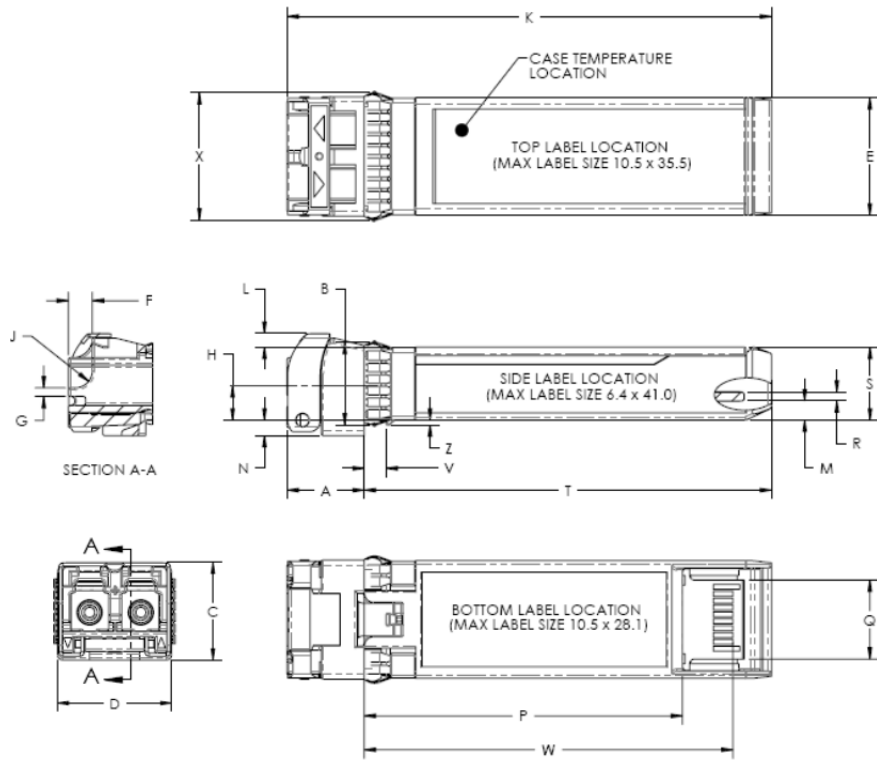


Figure 2. Mechanical Dimensions

Note: Default label position is on the top side



**XIII. PCB Layout and Bezel Recommendations**

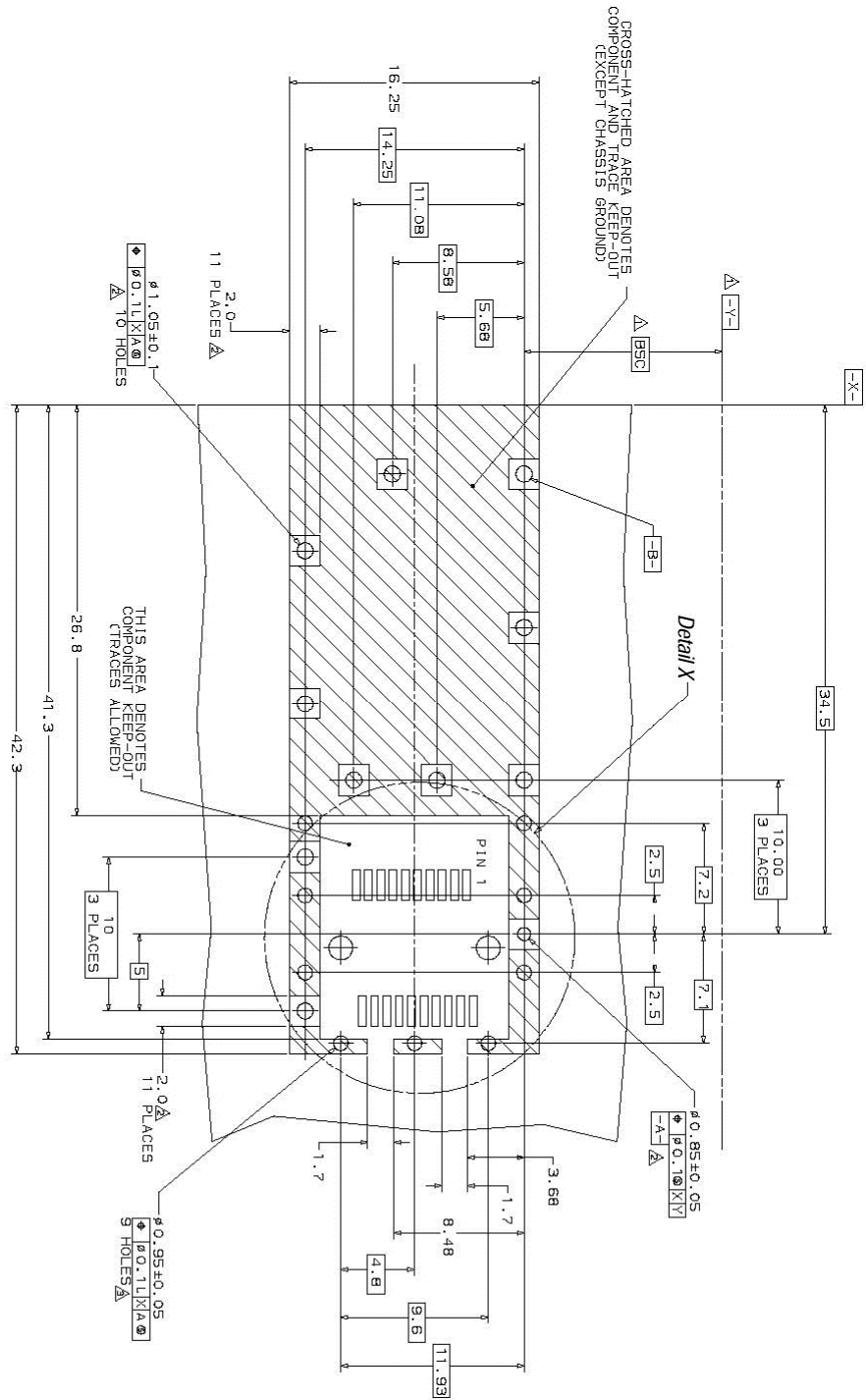
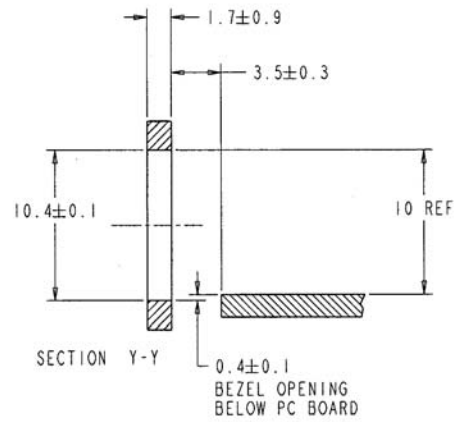
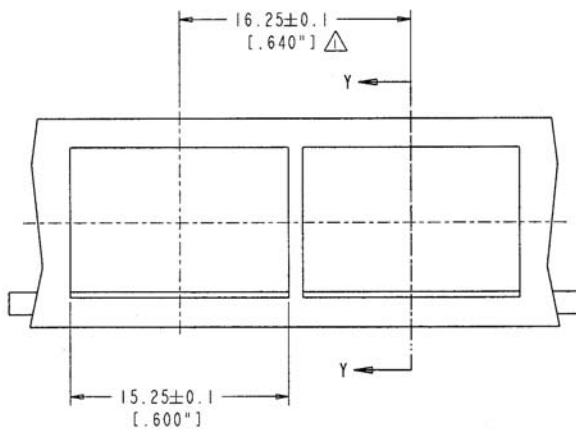
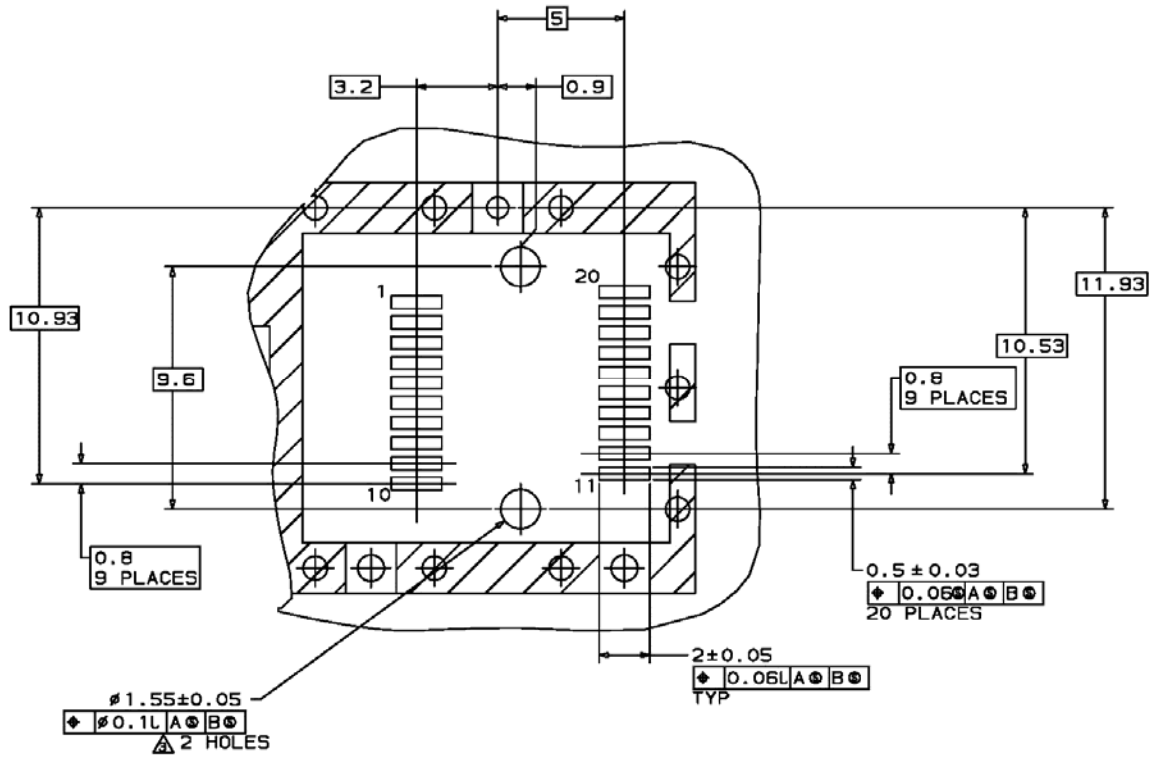


Figure 3. PCB Layout and Bezel Recommendations

- $\Delta$  Datum and Basic Dimension Established by Customer
- $\Delta$  Pads and Vias are Chassis Ground, 11 Places
- $\Delta$  Through Holes are Unplated



NOTES:

△ MINIMUM PITCH ILLUSTRATED, ENGLISH DIMENSIONS ARE FOR REFERENCE ONLY

2. NOT RECOMMENDED FOR PCI EXPANSION CARD APPLICATIONS

**XIV. References**

1. “Specifications for Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module ‘SFP+ ‘”, SFF Document Number SFF-8431, Revision 4.1, including SFF-8431 Rev 4.1 Addendum. September 15, 2013.
2. “Improved Pluggable Form factor”, SFF Document Number SFF-8432, Revision 4.2, April 18, 2007.
3. ITU-T G.693, VSR2000-2R1 Optical interface parameters specified for SONET/SDH applications with 2km target distance
4. IEEE 802.3ae, Clause 52, PMD Type 10GBASE-LR. IEEE Standards Department.
5. American National Standard for Information Technology - Fibre Channel - 10 Gigabit Fibre Channel, Rev 3.5, April 9, 2003.
6. “Digital Diagnostics Monitoring Interface for Optical Transceivers”. SFF Document Number SFF-8472, Revision 10.1, March 1, 2007.
7. Directive 2011/65/EU of the European Council Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment”, 08-June 2011, which supersedes the previous ROHS Directive 2002/95/EC.
8. “Application Note AN-2038: Finisar Implementation Of RoHS Compliant Transceivers”, Finisar Corporation, January 21, 2005.
9. ITU-T G.8251, The control of jitter and wander within the optical transport network (OTN)
10. Fibre Channel, Physical Interface-5, (FC-PI-5), REV 6.00, September 21, 2010

**XV. Revision History**

Revision	Date	Description
B1	1/7/2014	Production Release

**XVI. For More Information**

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